MGA-86563

0.5 – 6 GHz Low Noise GaAs MMIC Amplifier

Data Sheet

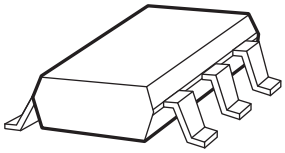
Description

Avago's MGA-86563 is an economical, easy-to-use GaAs MMIC amplifier that offers low noise figure and excellent gain for applications from 0.5 to 6 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of the SOT-143.

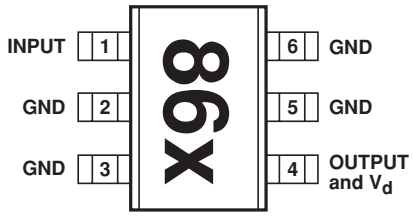
The MGA-86563 may be used without impedance matching as a high performance 2 dB NF gain block. Alternatively, with the addition of a simple shunt-series inductor at the input, the device noise figure can be reduced to 1.6 dB at 2.4 GHz. For 1.5 GHz applications and above, the output is well matched to 50 Ω. Below 1.5 GHz, gain can be increased by using conjugate matching.

The circuit uses state-of-the-art PHEMT technology with self-biasing current sources, a source-follower interstage, resistive feedback, and on-chip impedance matching networks. A patented, on-chip active bias circuit allows operation from a single +5 V power supply. Current consumption is only 14 mA, making this part suitable for battery powered applications.

Surface Mount Package
SOT-363 (SC-70)



Pin Connections and Package Marking



Note:
Package marking provides orientation and identification.
"86" = Device Code
"x" = Date code character identifies month of manufacture

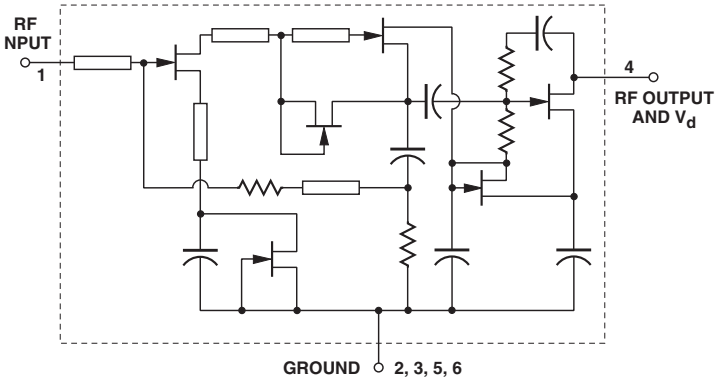
Features

- Lead-free Option Available
- Ultra-Miniature Package
- Internally Biased, Single +5 V Supply (14 mA)
- 1.6 dB Noise Figure at 2.4 GHz
- 21.8 dB Gain at 2.4 GHz
- +3.1 dBm P_{1dB} at 2.4 GHz

Applications

- LNA or Gain Stage for ISM, PCS, MMDS, GPS, TVRO, and Other C band Applications

Equivalent Circuit



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Human Body Model (Class 0)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

MGA-86563 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage, RF Output to Ground	V	9
V_{in}	RF Input Voltage to Ground	V	+0.5 –1.0
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]: $\theta_{ch\text{-}c} = 160°C/W$

Notes:

1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

Electrical Specifications, $T_C = 25°C$, $Z_0 = 50\ \Omega$ unless noted, $V_d = 5$ V

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G_{test}	Gain in Test Circuit[1]	f = 2.0 GHz		17	20	
NF_{test}	Noise Figure in Test Circuit[1]	f = 2.0 GHz			1.8	2.3
NF_O	Optimum Noise Figure	f = 0.9 GHz	dB		2.0	
	(Tuned for lowest noise figure)	f = 2.0 GHz			1.5	
		f = 2.4 GHz			1.6	
		f = 4.0 GHz			1.7	
		f = 6.0 GHz			2.0	
G_A	Associated Gain at NF_O	f = 0.9 GHz	dB		20.8	
	(Tuned for lowest noise figure)	f = 2.0 GHz			22.7	
		f = 2.4 GHz			22.5	
		f = 4.0 GHz			18.0	
		f = 6.0 GHz			13.7	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.9 GHz	dBm		3.6	
	(50 Ω Performance)	f = 2.0 GHz			4.1	
		f = 2.4 GHz			4.2	
		f = 4.0 GHz			4.3	
		f = 6.0 GHz			3.3	
IP_3	Third Order Intercept Point	f = 2.4 GHz	dBm		+15	
$VSWR_{in}$	Input VSWR	f = 2.4 GHz			2.3:1	
$VSWR_{out}$	Output VSWR	f = 2.4 GHz			1.7:1	
I_d	Device Current		mA		14	

Note:

1. Guaranteed specifications are 100% tested in the circuit in Figure 10 in the Applications Information section.

MGA-86563 Typical Performance, $T_c = 25°C$, $V_d = 5$ V

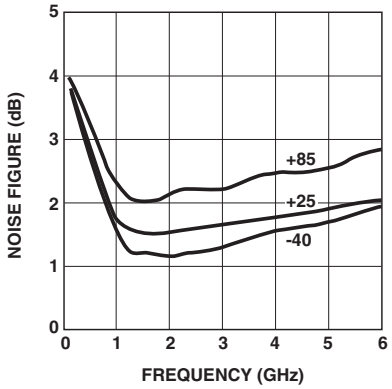


Figure 1. Minimum Noise Figure (Optimum Tuning) vs. Frequency and Temperature.

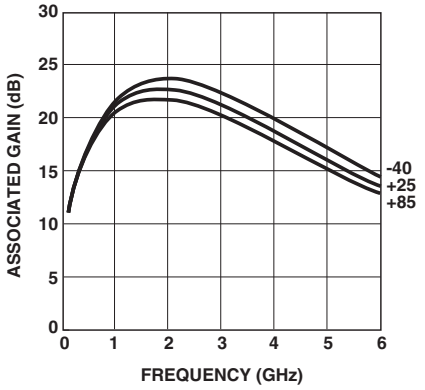


Figure 2. Associated Gain (Optimum Tuning) vs. Frequency and Temperature.

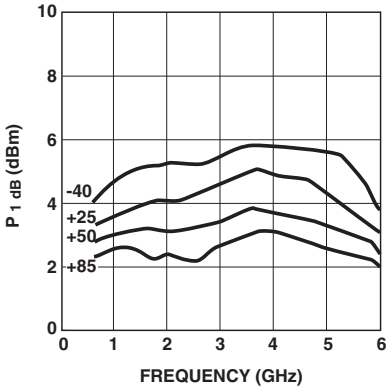


Figure 3. Output Power for 1 dB Gain Compression (into 50 Ω) vs. Frequency and Temperature.

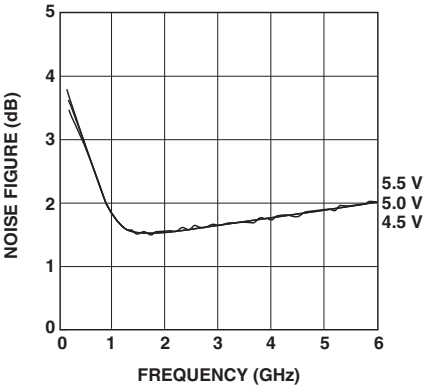


Figure 4. Minimum Noise Figure (Optimum Tuning) vs. Frequency and Voltage.

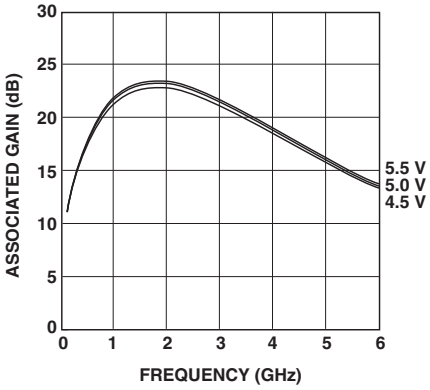


Figure 5. Associated Gain (Optimum Tuning) vs. Frequency and Voltage.

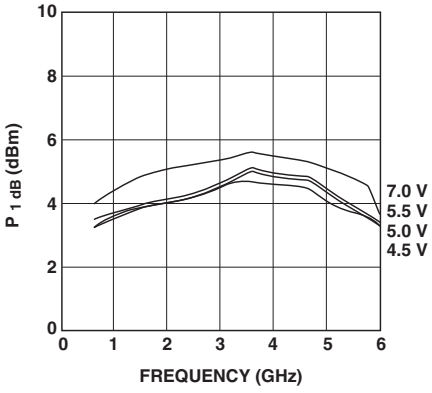


Figure 6. Output Power for 1 dB Gain Compression (into 50 Ω) vs. Frequency and Voltage.

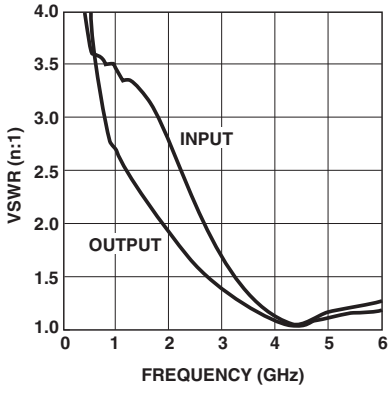


Figure 7. Input and Output VSWR (into 50 Ω) vs. Frequency.

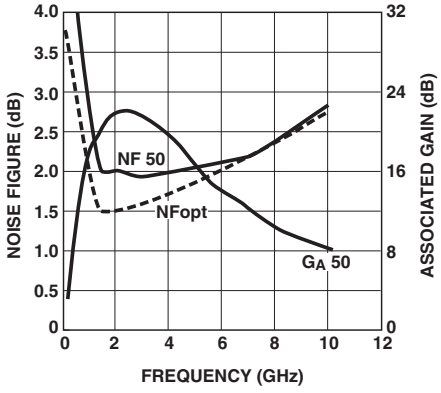


Figure 8. 50 Ω Noise Figure and Associated Gain vs. Frequency.

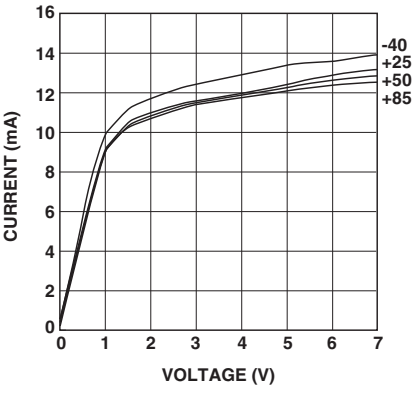


Figure 9. Device Current vs. Voltage.

MGA-86563 Typical Scattering Parameters[1], $T_C = 25°C$, $Z_0 = 50\ \Omega$, $V_d = 5\ V$

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Factor
0.1	0.84	-17	3.1	1.42	76	-39.8	0.010	15	0.85	-15	3.27
0.5	0.57	-29	14.7	5.41	41	-44.3	0.006	-23	0.59	-39	6.77
1.0	0.55	-41	18.9	8.77	4	-51.2	0.003	-2	0.46	-53	10.49
1.5	0.53	-57	20.8	10.97	-29	-52.1	0.002	70	0.38	-66	14.23
2.0	0.47	-73	21.7	12.14	-62	-45.2	0.005	96	0.32	-78	5.94
2.5	0.38	-89	21.8	12.33	-94	-40.7	0.009	102	0.24	-89	3.78
3.0	0.26	-104	21.3	11.61	-125	-37.4	0.014	100	0.16	-99	2.92
3.5	0.14	-115	20.2	10.23	-152	-34.4	0.018	97	0.09	-102	2.75
4.0	0.04	-106	18.8	8.75	-177	-32.6	0.023	92	0.03	-82	2.58
4.5	0.04	-6	17.4	7.44	162	-30.9	0.027	88	0.03	1	2.58
5.0	0.07	2	16.1	6.41	143	-29.6	0.032	83	0.05	20	2.53
5.5	0.09	-4	14.9	5.57	126	-28.1	0.038	78	0.06	19	2.45
6.0	0.11	-17	13.9	4.93	110	-26.0	0.044	72	0.08	14	2.38
6.5	0.12	-28	12.9	4.40	94	-24.9	0.050	65	0.08	4	2.35
7.0	0.13	-36	12.0	3.96	79	-23.8	0.057	59	0.09	-3	2.29
7.5	0.15	-44	11.1	3.58	65	-22.6	0.065	53	0.11	-12	2.21
8.0	0.17	-53	10.4	3.30	51	-22.6	0.074	44	0.13	-21	2.10

MGA-86563 Typical Noise Parameters[1], $T_C = 25°C$, $Z_0 = 50\ \Omega$, $V_d = 5\ V$

Frequency	NF_o			
(GHz)	(dB)	Mag.	Ang.	$R_N/50\ \Omega$
5	2.8	0.61	4	1.16
1.0	1.8	0.56	24	0.47
1.5	1.5	0.50	33	0.34
2.0	1.5	0.45	40	0.38
2.5	1.6	0.41	50	0.33
3.0	1.6	0.38	57	0.30
4.0	1.7	0.32	73	0.28
5.0	1.9	0.24	98	0.27
6.0	2.1	0.15	131	0.24

Note:

1. Reference plane per Figure 11 in Applications Information section.

MGA-86563 Applications Information

Introduction

The MGA-86563 is a high gain, low noise RF amplifier for use in wireless RF applications within the 0.5 to 6 GHz frequency range. The MGA-86563 is a three-stage, GaAs Microwave Monolithic Integrated Circuit (MMIC) amplifier that uses internal feedback to provide wideband gain and impedance matching.

A patented, active bias circuit makes use of current sources to "re-use" the drain current in all three stages of gain, thus minimizing the required supply current and decreasing sensitivity to variations in power supply voltage.

Test Circuit

The circuit shown in Figure 10 is used for 100% RF testing of Noise Figure and Gain. The input of this circuit is fixed tuned for a conjugate power match (maximum power transfer, or, minimum Input VSWR) at 2 GHz. Tests in this circuit are used to guarantee the NF_{test} and G_{test} parameters shown in the Electrical Specifications Table.

The 3.3 nH inductor, L1 (Coilcraft, Cary, IL or equivalent) in series with the input of the amplifier matches the input to 50Ω at 2 GHz.

The parameter test circuit uses a high impedance RF choke to apply V_d to the MMIC while isolating the power supply from the RF Output of the amplifier.

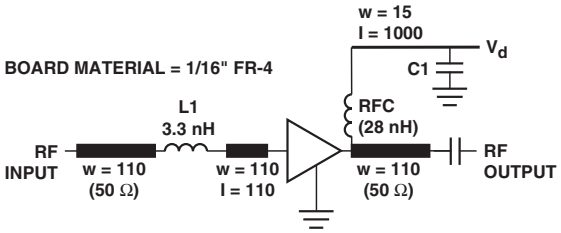


Figure 10. Test Circuit for 2 GHz.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters and to specify Γ_{opt} for the Noise Parameters are shown in Figure 11. As seen in the illustration, the reference planes are located at the extremities of the package leads.

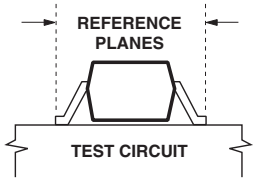


Figure 11. Reference Planes.

Biasing

The MGA-86563 is a voltage-biased device and operates from a single +5 volt power supply. With a typical current drain of only 14 mA, the MGA-86563 is suitable for use in battery powered applications. RF performance is very stable over a wide variation of power supply voltage.

Since DC bias is applied to the MGA-86563 through the RF Output pin, some method of isolating the RF from the DC must be provided. An RF choke or length of high impedance transmission line is typically used for this purpose.

SOT-363 PCB Layout

A PCB pad layout for the miniature SOT-363 (SC-70) package used by the MGA-86563 is shown in Figure 12 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the MGA-86563. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

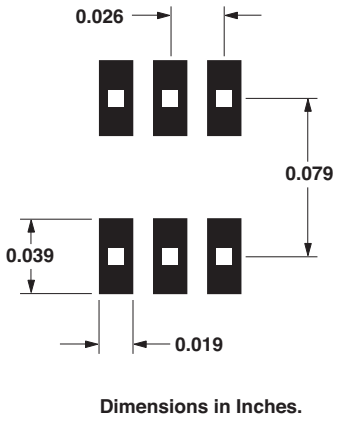


Figure 12. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.

RF Layout

The RF layout in Figure 13 is suggested as a starting point for amplifier designs using the MGA-86563 MMIC. Adequate grounding is needed to obtain maximum performance and to obviate potential instability. All four ground pins of the MMIC should be connected to RF ground by using plated through holes (vias) near the package terminals.

It is recommended that the PCB pads for the ground pins NOT be connected together underneath the body of the package. PCB traces hidden under the package cannot be adequately inspected for SMT solder quality.

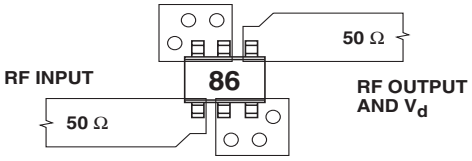


Figure 13. RF Layout.

PCB Material

FR-4 or G-10 printed circuit board material is a good choice for most low cost wireless applications. Typical board thickness is 0.020 or 0.031 inches. The width of 50Ω microstriplines in PC boards of these thicknesses is also convenient for mounting chip components such as the series inductor that is used at the input for impedance matching or for DC blocking capacitors.

For applications requiring the lowest noise figures, the use of PTFE/glass dielectric materials may be warranted to minimize transmission line losses at the amplifier input. A 0.5 inch length of 50Ω microstripline on FR-4 has approximately 0.3 dB loss at 4 GHz which will add directly to the noise figure of the MGA-86563.

Typical Application Circuit

A typical implementation of the MGA-86563 as a low noise amplifier is shown in Figure 14.

A 50Ω microstripline with a series DC blocking capacitor, C1, is used to feed RF to the MMIC. The input of the MGA-86563 is already partially matched for noise figure and gain to 50Ω. The use of a simple input matching circuit, such as a series inductor, will minimize amplifier noise figure. Since the impedance match for NF_O (minimum noise figure) is very close to a conjugate power match, a low noise figure can be realized simultaneously with a low input VSWR.

DC power is applied to the MMIC through the same pin that is shared with the RF output. A 50Ω microstripline is used to connect the device to the following stage. A bias decoupling network is used to feed in V_d while simultaneously providing a DC block to the RF signal. The bias decoupling network shown in Figure 14, consisting of resistor R1, a short length of high impedance microstripline, and bypass capacitor C3, will provide excellent performance over a wide frequency range. Surface mount chip inductors could be used in place of the high impedance transmission line to act as an RF choke. Consideration should be given to potential resonances and signal radiation when using lumped inductors.

For operation at frequencies below approximately 2 GHz, the addition of a simple impedance matching circuit to the output will increase the gain and output power by 0.5 to 1.5 dB. The output matching circuit will not effect the noise figure.

A small value resistor placed in series with the V_{dd} line may be useful to "de-Q" the bias circuit. Typical values of R1 are in the 10 Ω to 100 Ω range. Depending on the value of resistance used, the supply voltage may have to be increased to compensate for voltage drop across R1. The power supply should be capacitively bypassed (C3) to ground to prevent undesirable gain variations and to eliminate unwanted feedback through the bias lines that could cause oscillation.

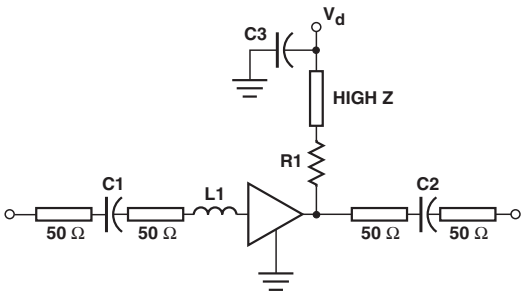


Figure 14. Typical Amplifier Circuit.

Higher Bias Voltages

While the MGA-86563 is designed primarily for use in +5 volt applications, the internal bias regulation circuitry allows it to be operated with any power supply voltage from +5 to +7 volts. The use of +7 volts increases the P_{1dB} by approximately 1 dBm. The effect on noise figure, gain, and VSWR with higher V_d is negligible.

For more information call your nearest Avago sales office.

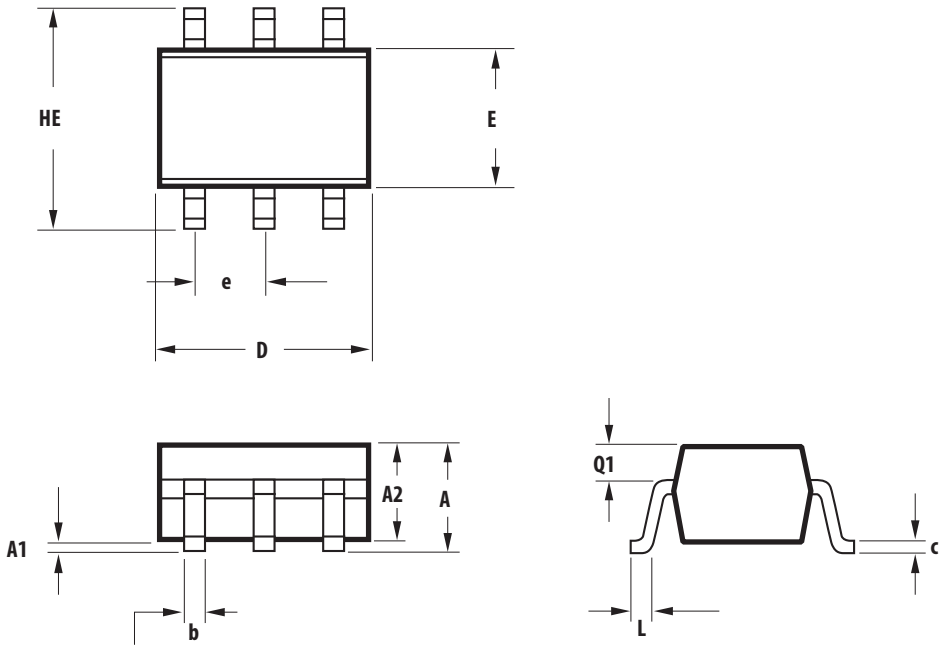
Part Number Ordering Information

Part Number	No. of Devices	Container
MGA-86563-TR1	3000	7" Reel
MGA-86563-TR2	10000	13" Reel
MGA-86563-BLK	100	antistatic bag
MGA-86563-TR1G	3000	7" Reel
MGA-86563-TR2G	10000	13" Reel
MGA-86563-BLKG	100	antistatic bag

Note: For lead-free option, the part number will have the character "G" at the end.

Package Dimensions

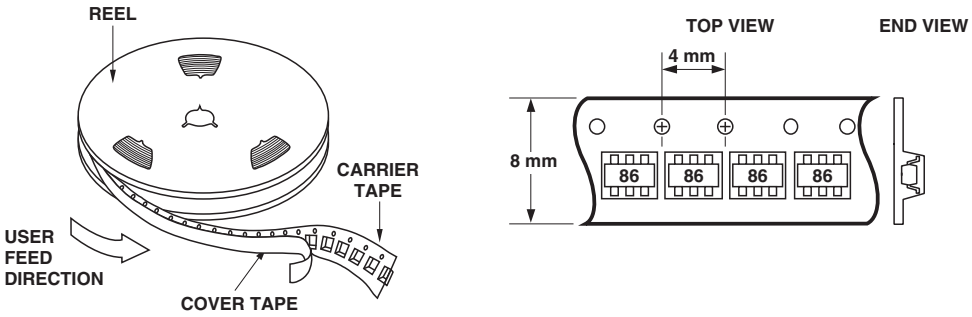
Outline 63 (SOT-363/SC-70)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
Q1	0.10	0.40
e	0.650 BCS	
b	0.15	0.30
c	0.10	0.20
L	0.10	0.30

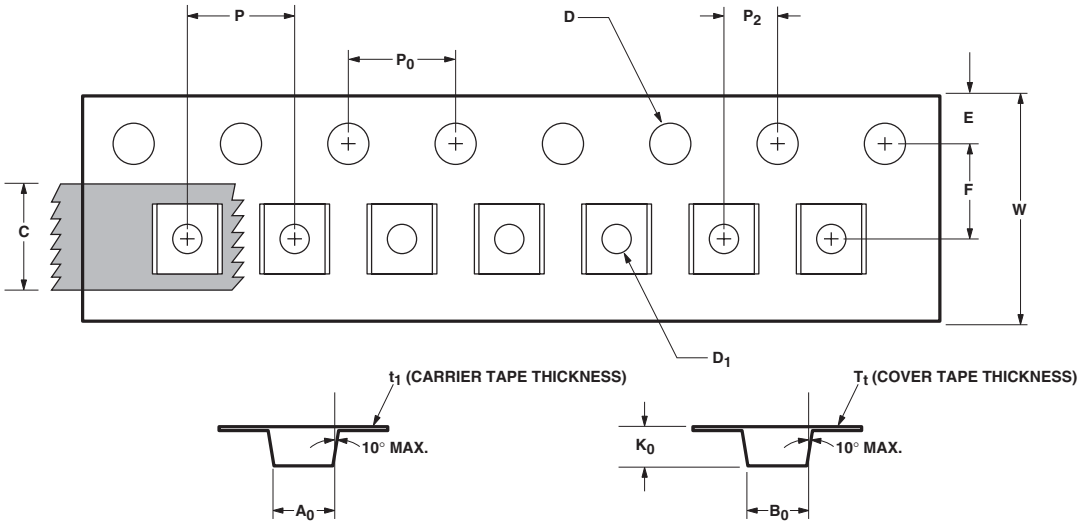
NOTES:
1. All dimensions are in mm.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to EIAJ SC70.
5. Die is facing up for mold and facing down for trim/form, ie: reverse trim/form.
6. Package surface to be mirror finish.

Device Orientation



Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.10	0.061 + 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.40 ± 0.10	0.205 + 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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